

AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Please replace paragraph [0032] beginning on page 8 of the Specification with the following amended paragraph:

---[0032] The command processing unit 11 has an address conversion unit 100, as shown in FIG. 2, and a function for converting a logical address to a physical address. Specifically, the address conversion unit 100 converts addresses so that, in the case where a rectangular area of M pixels \times N lines (M and N are integers) in the image data is accessed, the column address of data in a $(K+m)$ th line (K and m are integers and $m \leq M$) of an L th (L is an integer) line and the column address of data at the K th column of a $(L+n)$ th line (L and n are integers and $n \leq N$) become successive. FIG. 3 is an example of the mapping performed in conventional address conversion; in the case where the minimal access size of the DRAM is 4 bursts, data at one part of a $(K+1)$ th column and all data at $(K+2)$ th and $(K+3)$ th columns become invalid data and the effective bandwidth drops. On the other hand, FIG. 4 is an example of mapping performed in the address conversion unit 100, when $[m=2]$ $m=1$ and $n=1$. By making the column address of data in the $(K+1)$ th column address and the column address of data in the $(K+2)$ th column address successive, only a part of data in the $(K+1)$ th column and a part of data in the $(K+2)$ th column are wastefully transferred. In FIG. 5, an example of the logical and physical address conversion in the address conversion unit 100 is shown.---

Please replace paragraph [0033] beginning on page 9 of the Specification with the following amended paragraph:

---[0033] FIG. 6 is an example of the mapping of the address conversion unit 100 when $[[m=2]]$ $m=1$ and $n=2$.

In FIG. 6, the addresses are successive in the sequence: Lth line, (L+2)th line, (L+1)th line, (L+3)th line. When the minimum access size of the DRAM is 4 bursts, in the first access, the Lth line and (L+2)th line are accessed, and in the second access, the (L+1)th line and the (L+3)th line are accessed. For example in motion compensation processing, when the field is estimated, the access is performed by skipping a line of the reference image. Once mapping is performed as in FIG. 6, when field estimation is performed in motion compensation processing, the invalid transfer load is reduced and it becomes possible to improve the effective bandwidth. Also, when the frame is estimated, access to the lines circled 1 and circled 2 as in FIG. 6 may be repeated with no problems.-

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